Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.073”**

**V OUT**

**ADJ**

**V IN**

**V OUT**

**MASK**

**REF**

**AA**

**80B**

**.047”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 80B**

**APPROVED BY: DK DIE SIZE .047” X .073” DATE: 11/11/21**

**MFG:NATIONAL SEMI THICKNESS .010” P/N: LM337L**

**DG 10.1.2**

#### Rev B, 7/19/02